Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please amend the claims as follows:

1. (currently amended) A flip-flop comprising:

a first latch for receiving at least one bit;

a second latch coupled to the first latch for storing the at least one bit from the first latch, wherein the size of the second latch is minimized compared to the size of the first latch to reduce power consumption; and

a multiplexor coupled to the first latch and to the second latch for outputting the at least one bit from the first latch when a first clock to the first latch is active and for outputting the at least one bit from the second latch when a second clock to the second latch is active.

2. (original) The flip-flop of claim 1 wherein the multiplexor is a shunt multiplexor.

3. (original) The flip-flop of claim 1 wherein a first clock causes the at least one bit to be provided from the first latch to the multiplexor and the second latch.

4. (original) The flip-flop of claim 1 wherein the first latch is a master latch.

5. (original) The flip-flop of claim 3 wherein the second latch is a slave latch.

6. (currently amended) A flip-flop comprising:

a master latch for receiving at least one bit;

a slave latch coupled to the master latch for storing the at least one bit from the master latch wherein the size of the slave latch is minimized compared to the size of the master latch to reduce power consumption; and

a multiplexor coupled to the master latch and to the slave latch for outputting the at least one bit from the master latch when a first clock to the master latch is active and for outputting the at least one bit from the slave latch when a second clock to the slave latch is active.

7. (previously amended) The flip-flop of claim 6 wherein a first clock causes the at least one bit to be provided from the master latch to the multiplexor and the slave latch.

8. (previously amended) A method for optimizing power and performance in a flip-flop, wherein the flip-flop includes a first latch and a second latch coupled to the first latch, the method comprising the steps of:

(a) receiving at least one bit into the first latch, wherein the first latch outputs the at least one bit to the second latch and to a multiplexor when a first clock to the first latch is active;

(b) outputting the at least one bit received from the first latch from the multiplexor when the first clock is active; and

(c) outputting the at least one bit received from the second latch from the multiplexor when a second clock to the second latch is active.

9. (currently amended) A flip-flop comprising:

a master latch for receiving at least one bit;

a slave latch coupled to the master latch for storing the at least one bit, wherein the size of the ~~second~~ master latch is minimized compared to the size of the master latch to reduce power consumption; and

a shunt multiplexor coupled to the master latch and to the slave latch for receiving the at least one bit, for outputting the at least one bit from the master latch when a first clock to the master latch is active, and for outputting the at least one bit from the slave latch when a second clock to the slave latch is active.

10. (previously added) A flip-flop comprising:

a first latch for receiving at least one bit;

a second latch coupled to the first latch for storing the at least one bit from the first latch, wherein the size of the second latch is smaller than the size of the first latch to reduce power consumption; and

a multiplexor coupled to the first latch and to the second latch for outputting the at least one bit from the first latch when a first clock to the first latch is active and for outputting the at least one bit from the second latch when a second clock to the second latch is active.